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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,252	CSONKA ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-59* is/are pending in the application.

4a) Of the above claim(s) *12-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37,38,41-45,48-50,53 and 56-59* is/are rejected.

7)☒ Claim(s) *39,40,46,47,51,52,54 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0105//31 Jan 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 37-59 in the reply filed on June 16, 2005 is acknowledged. Claims 12-36 have been withdrawn from consideration. Accordingly, Claims 37-59 have received a first action on the merits hereinbelow.

Claim Objections

2. Claim 37 is objected to because of the following informalities:

In Claim 37, line 5: "said digital circuit" has no antecedent basis. This defect may be overcome by changing the phrase in the preamble as "The apparatus for a signal-triggered digital memory system device" to –The apparatus for a signal-triggered digital circuit of a memory system device--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 48 and 59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A) As to Claim 48:

In base Claim 37, the "input receiver is located within said memory device" and "said conducting signal path being electrically connected to said conducting interface, said conducting interface being electrically connected to said input receiver." In dependent Claim 42, there is "a circuit substrate, wherein said conducting interface and said conducting signal path are located on said circuit substrate." In Claim 48, there is recited "**a memory module on which said memory device is located**" (bold emphasis added). Since the above-cited recitations in base Claim 37 require that the memory device is located on the memory module, the input receiver is located within the memory device and the conducting interface is electrically connected to the input receiver, **AND** the above-cited recitation in dependent Claim 42 requires that the conducting interface and signal path are located on the circuit substrate, then "said circuit substrate" of dependent Claim 48 (depending from Claims 42 and 37) CANNOT BE THE SAME CIRCUIT SUBSTRATE of Claim 42 because **the circuit substrate** of Claim 42, on which is located the "conducting interface" and, from Claim 37, the memory device including the input receiver therein, **MUST** be **a structural component of the memory module**. So the "circuit substrate" comprising "a slot" into which the memory module (with the memory device that includes the input receiver and the conducting interface and conducting signal path) is connected by way of the memory module edge connector.

Therefore, "said circuit substrate" of dependent Claim 48 is ***not the same*** *"circuit substrate" of Claim 42; rather, it is a newly introduced circuit substrate (such as a*

motherboard with slot connectors) for receiving the edge connector of the ***memory module circuit substrate*** *of Claim 42.*

B) As to Claim 59, there is no antecedent basis for "said memory system" in line 2 and it is not possible, for reasons similar to those explained in the rejection to Claim 48, above, that the circuit substrate of Claim 59 is the same as the circuit substrate of Claim 58 because the circuit substrate of Claim 58 MUST be the "memory module" on which the "memory device" is located, the "memory device" having the "input receiver" that is connected to the "conducting interface" (all recited in base Claim 49). Therefore, the "circuit substrate" of Claim 59, comprising "a slot" to which the "edge connector" of the "memory module" is connected, is some other circuit board, such as a motherboard with connector slot in which the edge connector of the circuit board memory module of Claim 58 is connected.

Rejections Based On Prior Art

5. The following references were relied upon for the rejections hereinbelow:

Jonaidi (US 6,091,155) Akram (US 6,008,538)

Sanwo et al. (US 5,530,623)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 37, 38, 41-45, 49, 50, 53 and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al.

A) As to Claim 37:

I. Jonaidi discloses, in Fig. 2, an apparatus of a signal-triggered electronic device digital circuit, the apparatus comprising: a controller signal source for generating a digital control signal (col.1: 10-17); an input receiver (IC chip; col.1: 10-17) within the electronic device, the input receiver receiving the digital signal for the digital circuit and being responsive to triggering induced by the digital circuit (col.1: 10-17); a conducting interface 38; a conducting signal path 40, the conducting signal path 40 being electrically connected to the conducting interface 38, the conducting interface 38 being connected to the input receiver (the input receiver--IC chip--is surface mounted through bump 52 on the conducting interface 38; Figs. 2 and 7 and col.8: 43-47), the signal path 40 carrying the digital signal thereover (col.1: 10-17 and col.5: 29-31); and wherein the

conducting interface 38 is substantially rectangular in planar view (Fig. 2 and col.5: 27-29) and the conducting signal path 40 connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of conducting interface 38 to which the conducting signal path 40 is connected (Fig. 2 and col.5: 36-38); i.e., since rectangular conducting interface 38 is approximately 26 mils on each side, then conducting interface 38 is a square, being a special case of the rectangle. Note that in Fig. 2, the center of the square conducting interface 38, its corner and the center of the via 36 are collinear and coincident with the longitudinal centerline axis of conducting signal path 40, distinct from the non-collinear embodiments of Figs.3-5, as pointed out by Jonaidi in col.7: 5-28 (wherein Jonaidi describes the embodiment of Fig. 3 as being distinct from the embodiment of Fig. 2 in that the center of square conducting interface 38, the corner of square conducting interface 38 and the center of via 36 are not collinear). Now, from geometry it is known that a diagonal of a square includes the center of the square and forms a 45 degree angle with the sides. Accordingly, the supplemental angle formed between the longitudinal centerline axis of conducting signal path 40--which lies coincident with the diagonal of the square pad 38--and the side of the square pad 38 is 135 degrees; i.e., within a range of 110 to 160 degrees.

II. Jonaidi discloses control signal sources and input receivers (IC chips) for general purpose use in computers (col.1: 10-17) and does not specify the type of controller and the type of electronic device within which is located the input receiver (IC chip) and the digital circuit for a specific application.

III. Sanwo et al. discloses a memory device digital circuit (Fig. 2) comprising a memory controller 17 for controlling the input receivers (memory IC chips 43) mounted on cards 31-38 in connectors 21-28 on motherboard 15, the cards 31-38 being memory modules having conducting interfaces for receiving the input receivers (chips 43) and conducting signal paths for carrying the digital signals to and from the memory controller 17.

IV. Since Jonaidi discloses control signal sources and IC chips for general purpose use in computers, the use of memory IC chips in a memory device in a computer system and a memory controller to manage the read/write memory functions in the computer system, as taught by Sanwo et al., would have been readily recognized as one of the applications of the land pattern and IC mounting system contemplated in col.1: 10-17 of Jonaidi.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the controller and input receiver (IC chip) of Jonaidi et al. with the memory controller and memory chip of Sanwo et al. in order to provide a computer system with a memory system, as taught by Sanwo et al., using the effective solder-mounting of the IC chip on the conductive interface taught by Jonaidi, on the memory module of Sanwo et al.

VI. Since parts I-V establish the **structure** of the claim, the **functional limitation** "thereby to produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees" is an inherent property of the

connection at an angle of 135 degrees between the conducting interface 38 and the conducting signal path 40 disclosed in the structure of Jonaidi.

B) As to Claim 38, modified Jonaidi further discloses the conducting signal path 40 is connected to the conducting interface 38 at a corner thereof (Fig. 2).

C) As to Claim 41, modified Jonaidi further discloses the angle in a range of 110 to 160 degrees is an angle of 135 degrees (see analysis in part I of the rejection of Claim 37, above).

D) As to Claim 42, modified Jonaidi further discloses a circuit substrate 32 (this **circuit substrate 32** corresponds to **the memory module package 31** of Sanwo et al., upon which the input receiver--IC chip 43--is mounted; specifically, mounted on the conducting interface of said memory module/circuit substrate, as established in the rejection of base Claim 37, above), wherein conducting interface 38 and conducting signal path 40 are located on the circuit substrate 32 (Fig. 2 and col.5: 14-16).

E) As to Claim 43, modified Jonaidi further discloses the circuit substrate 32 comprises a printed circuit board (col.5: 14-16) and wherein conducting interface 38 is a pad and conducting signal path 40 is a trace (Fig. 2 and col.5: 27-31).

F) As to Claim 44, modified Jonaidi further discloses pad 38 is substantially square in planar view (Fig. 2 and col.5: 36-38).

G) As to Claim 45:

Modified Jonaidi discloses trace 40 has a width of approximately 6 mils (Fig. 2 and col.5: 41-43) and pad 38 has a width of 26 approximately mils (Fig. 2 and col.5: 36-38). So Jonaidi teaches, in Fig. 2, an exemplary land pattern 30 wherein the width of

trace 40 is greater than 1/5th of a width of pad 38 to which trace 40 is connected (i.e., 6 mil ÷ 26 mil = 0.23 > 1/5th). However, **Jonaidi further teaches that the exemplary dimensions in Fig. 2 can be varied in the disclosed land pattern 30 (col.5: 44-47)**. Therefore, in order to provide the pad 38 with a size sufficient to accommodate the necessary solder without exhibiting the "pullback" phenomenon, as well as to solve other printed circuit and solder mounting problems disclosed in the Background (cols. 1-3), and to accommodate the pitch densities and wire routing layout requirements of a particular circuit board packaging application, it would have been an obvious matter of engineering choice, as suggested by Jonaidi in col.5: 44-47, to optimize the required pad and wiring pitch densities and layout configuration appropriate for each application of the disclosed land pattern 30 of Fig. 2, in accordance with package dimension, cost and other spatial and mechanical packaging process and finished-product requirements for that application. Furthermore, and consistent with the teaching of Jonaidi in col.5: 44-47, and the above-mentioned optimizing of wiring pad and wiring pitch densities, layout configuration, cost and other packaging dimension and spatial and mechanical considerations for the particular application, as suggested in the col.5: 44-47 teaching of Jonaidi, it has been held that discovering an optimum value of a result effective variable [in this case, the trace to pad width ratio of **exactly** 1/5th in Claim 45] involves only routine skill in the art. *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

H) As to Claim 49:

I. Jonaidi discloses, in Fig. 2, a circuit substrate 32 for a signal-triggered electronic device digital circuit, the circuit substrate 32 comprising: a conducting

interface 38, substantially rectangular in planar view, for electrical connection to an input receiver (the input receiver--IC chip--is surface mounted through bump 52 on the conducting interface 38; Figs. 2 and 7 and col.8: 43-47) of a digital circuit, the input receiver receiving a digital control signal over the digital circuit (col.1: 10-17) and being responsive to triggering induced by the digital circuit (col.1: 10-17); a conducting signal path 40, the conducting signal path 40 being electrically connected to the conducting interface 38, the conducting interface 38 being connected to the input receiver, the signal path 40 carrying the digital signal thereover (col.1: 10-17 and col.5: 29-31); and wherein the conducting interface 38 is substantially rectangular in planar view (Fig. 2 and col.5: 27-29) and the conducting signal path 40 connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of conducting interface 38 to which the conducting signal path 40 is connected (Fig. 2 and col.5: 36-38); i.e., since rectangular conducting interface 38 is approximately 26 mils on each side, then conducting interface 38 is a square, being a special case of the rectangle. Note that in Fig. 2, the center of the square conducting interface 38, its corner and the center of the via 36 are collinear and coincident with the longitudinal centerline axis of conducting signal path 40, distinct from the non-collinear embodiments of Figs.3-5, as pointed out by Jonaidi in col.7: 5-28 (wherein Jonaidi describes the embodiment of Fig. 3 as being distinct from the embodiment of Fig. 2 in that the center of square conducting interface 38, the corner of square conducting interface 38 and the center of via 36 are not collinear). Now, from geometry it is known that a diagonal of a square includes the center of the square and forms a 45 degree

angle with the sides. Accordingly, the supplemental angle formed between the longitudinal centerline axis of conducting signal path 40--which lies coincident with the diagonal of the square pad 38--and the side of the square pad 38 is 135 degrees; i.e., within a range of 110 to 160 degrees.

II. Jonaidi discloses control signal sources and input receivers (IC chips) for general purpose use in computers (col.1: 10-17) but does not specify the type of electronic device within which is located the input receiver (IC chip), and does not specify the type of digital circuit for a specific application.

III. Sanwo et al. discloses a memory device digital circuit (Fig. 2) comprising a memory controller 17 for controlling the input receivers (memory IC chips 43) mounted on memory module circuit substrates 31-38 in connectors 21-28 on motherboard 15, the circuit substrates 31-38 being memory modules having conducting interfaces for receiving the input receivers (chips 43) and conducting signal paths for carrying the digital signals to and from the memory controller 17.

IV. Since Jonaidi discloses control signal sources and IC chips for general purpose use in computers, the use of memory IC chips in a memory device in a computer system and a memory controller to manage the read/write memory functions in the computer system, as taught by Sanwo et al., would have been readily recognized as one of the applications of the land pattern and IC mounting system contemplated in col.1: 10-17 of Jonaidi.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the input receiver (IC chip) of Jonaidi et al. with

the memory chip of Sanwo et al. in order to provide a computer system with a memory device digital circuit, as taught by Sanwo et al., using the effective solder-mounting of the IC chip on the conductive interface taught by Jonaidi, on the memory module of Sanwo et al.

VI. Since parts I-V establish the **structure** of the claim, the **functional limitation** "thereby to produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees" is an inherent property of the connection at an angle of 135 degrees between the conducting interface 38 and the conducting signal path 40 disclosed in the structure of Jonaidi.

VII. Jonaidi discloses that conductive signal path 40 has a width of approximately 6 mils (Fig. 2 and col.5: 41-43) and pad 38 has a width of 26 approximately mils (Fig. 2 and col.5: 36-38). So Jonaidi teaches, in Fig. 2, an exemplary land pattern 30 wherein the width of signal path 40 is greater than $1/5^{th}$ of a width of pad 38 to which signal path 40 is connected (i.e., 6 mil ÷ 26 mil = 0.23 > $1/5^{th}$). However, **Jonaidi further teaches that the exemplary dimensions in Fig. 2 can be varied in the disclosed land pattern 30 (col.5: 44-47)**. Therefore, in order to provide the conducting interface 38 with a size sufficient to accommodate the necessary solder without exhibiting the solder "pullback" phenomenon (col.2: 57-col.3: 18), as well as to solve other printed circuit and solder mounting problems disclosed in the Background (cols.1-3), and to accommodate the pitch densities and wire routing layout requirements of a particular circuit board packaging application, it would have been an obvious matter of engineering choice, as

suggested by Jonaidi in col.5: 44-47, to optimize the required pad and wiring pitch densities and layout configuration appropriate for each application of the disclosed land pattern 30 of Fig. 2, in accordance with package dimension, cost and other spatial and mechanical packaging process and finished-product requirements for that application. Furthermore, and consistent with the teaching of Jonaidi in col.5: 44-47, and the above-mentioned optimizing of wiring pad and wiring pitch densities, layout configuration, cost and other packaging dimension and spatial and mechanical considerations for the particular application, as suggested in the col.5: 44-47 teaching of Jonaidi, it has been held that discovering an optimum value of a result effective variable [in this case, the conducting signal path to conducting interface width ratio of **exactly** $1/5^{th}$ in Claim 49] involves only routine skill in the art. *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

I) As to Claim 50, modified Jonaidi further discloses conductive interface 38 is substantially square in planar view (Fig. 2 and col.5: 36-38).

J) As to Claim 53, modified Jonaidi further discloses the conducting signal path 40 is connected to the conducting interface 38 at a corner thereof (Fig. 2).

K) As to Claim 56, modified Jonaidi further discloses the angle in a range of 110 to 160 degrees is an angle of 135 degrees (see analysis in part I of the rejection of Claim 37, above).

L) As to Claim 57, modified Jonaidi further discloses the circuit substrate 32 comprises a printed circuit board (col.5: 14-16) and wherein conducting interface 38 is a pad and conducting signal path 40 is a trace (Fig. 2 and col.5: 27-31).

M) As to Claim 58:

I. Jonaidi, as modified by Sanwo et al., does not teach that circuit substrate 32 (the memory module 31 in Sanwo et al.) comprises a signal source for generating the digital control signal; rather, the digital control signal is generated by an off-module signal source: i.e., the memory controller 17 of Sanwo et al.

II. However, Jonaidi teaches that there are other digital signal sources that can be mounted on the same board as the input receiver IC chip other than a memory controller (col.1: 10-17), such as a processor or ASIC as a source of some specific software or firmware instructions sent as digital signals. Therefore, in addition to the memory controller source of digital signals on the motherboard of Sanwo et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the circuit substrate 32 of Jonaidi to include another source of digital signals, such as a processor or ASIC to send data and instructions in the form of digital signals along the signal path 40 to the input receiver IC chip to perform electronic functions required by the application.

9. Claims 48 and 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al., as applied to claim 42, above, and further in view of Akram et al.

As to Claims 48 and 59 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection of the claims, above):

I. Jonaidi, as modified by Sanwo et al. discloses **a motherboard circuit substrate** (motherboard 15 in Fig. 2 of Sanwo et al.) comprising a slot (connector 21)

wherein the memory system further comprises a memory module, say module 31, on which the memory device 43 is located, the memory module 43 being a SIMM (col.1: 18-22; col.6: 6) comprising an edge connector 51 (Fig. 1 and col.3: 15-16), the SIMM being connected to memory controller 17 by edge connector 51 to slot 21 (col.2: 66-col.3: 3).

II. Jonaidi, as modified by Sanwo et al., does not teach the memory module (31 in Sanwo et al.) is a DIMM (dual in-line memory module); rather, memory module 31 is disclosed as a SIMM (single in-line memory module).

III. Akram et al. teaches that SIMM and DIMM devices are known in the art and that, in applications requiring greater memory than can be provided by a SIMM, DIMM devices are used instead (col.1: 31-43).

IV. Therefore, since both Akram et al. and Jonaidi as modified by Sanwo et al., are in a memory device application, then replacing the SIMM 31 of Jonaidi as modified by Sanwo et al. with the DIMM of Akram et al. would have been readily recognized as obvious to one of ordinary skill in the art at the time the invention was made in order to provide and increased memory capability for an application requiring greater memory capacity.

Allowable Subject Matter

10. Claims 39-40, 46, 47, 51, 52 and 54-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 39-40, patentability resides in the limitation wherein *the conducting signal path has a length which is at least 1/6th of a transition electrical length of the digital signal carried thereover*, in combination with the other limitations of the broadest claim, Claim 39.

As to Claims 46, patentability resides in the limitation wherein *the trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of the pad to which the trace is connected, in combination with the other limitations of the claim.*

As to Claim 47, patentability resides in the exact widths and thicknesses of the pad and trace as recited in the claim, in combination with the other limitations of the claim.

As to Claims 51, patentability resides in the limitation wherein *the conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the pad to which the conducting signal path is connected*, in combination with the other limitations of the claim.

As to Claim 52, patentability resides in *the exact widths and thicknesses of the conducting interface and the conducting signal path as recited in the claim*, in combination with the other limitations of the claim.

As to Claims 54-55, patentability resides in the limitation wherein *the conducting signal path has a length which is at least 1/6th of a transition electrical length of the*

digital signal carried thereover, in combination with the other limitations of the broadest claim, Claim 54.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Lichtblau (US 4,021,705) discloses, in Fig. 15, a side of the circuit substrate opposite the loop circuit in Fig. 14, wherein a signal path 74 connects two rectangular conducting interfaces (pads) 62 and 72 at the corners of the pads and at an angle that appears to be between 110 degrees and 160 degrees (Fig. 15 and col.6: 1-11).

b) Nishihara et al. (US 4,785,141) discloses, in Fig. 1A, a signal path 3 directly connected to a rectangular pad at the corner and at an angle that appears to be between 110 degrees and 160 degrees.

c) Dowsing, III et al. (5,541,565) discloses impedance matching by means of a widened portion 48 of a signal path 40 (Figs. 2 and 4; col.4: 59-col.5: 8).

d) Bree et al. (US 5,444,187) discloses a prior art solution to the loss problem on a signal path by using different angled turns in the signal path instead of 90 degree angled turns (col.4: 14-col.5: 49) and a solution that solves some problems with the prior art solution (col.8: 50-col.6: 15) and that comprises signal paths that include angles between the trace and the edge of the component between 0 and 180 degrees (Figs. 5-8; col.6: 61-col.9: 43).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
August 26, 2005